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SPECIFICATION

TITLE

"AN INTERMEDIATE BASE FOR A SEMICONDUCTOR MODULE, A SEMICONDUCTOR MODULE USING THE INTERMEDIATE BASE ~~AND A METHOD FOR PRODUCING THE INTERMEDIATE BASE~~"

BACKGROUND OF THE INVENTION

The present invention relates to an intermediate base for a module having at least one semiconductor component. The base comprises a flat base body having an upper face on which internal connections are formed for connection to connecting elements of the semiconductor component, a lower face, which is provided with external connections for making contact with a circuit base, carrier or board and through-holes extending between the upper face and the lower face, whose walls are at least partially metallized to make connections between the internal connections on the upper face and the corresponding external connections on the lower face. The invention also relates to the semiconductor module produced using this intermediate base and to the method for producing the intermediate base.

The increasing miniaturization of integrated circuits has led to the problem that an even greater number of electrical connections need to be accommodated in a very confined space between the actual semiconductor and the circuit carrier or base, that is to say the printed circuit board. However, the finer the structures of the semiconductor chip and of the connecting conductors, the greater is the extent to which they are at risk from different expansion levels of the materials involved, in particular the semiconductor body and the printed circuit board, which is composed of plastic.

The intermediate base or interposer plays a great role in making contact with a semiconductor chip. It allows one or more chips to be connected to form a module, with which contact is then made on the circuit carrier or board.

In the case of what is referred to as a BGA (Ball Grid Array) technology, an intermediate base is provided over the area of its lower face with solder studs, which allow surface mounting on a printed circuit board. The solder studs are, in this case, first used as electrical connections and secondly are used as spacers to compensate for expansion between the different materials of the intermediate base and printed circuit board. The conductor chip can be mounted on the upper face of the intermediate base, and contact can be made with it, for example, by means of bonding wires. Flip chip mounting is also known, in which the connections of the unhoused semiconductor are directly connected to conductor tracks on the upper face of the intermediate base. In order to provide expansion compensation between the semiconductor body and the intermediate base in this case, underfilling is generally required for the semiconductor, which involves the necessity for additional, complicated and expensive processing steps, which also do not allow subsequent repair.

In the case of what is referred to as PSGA (Polymer Stud Grid Array) technology, the injection-molded, three-dimensional substrate composed of an electrically insulating polymer is used as the intermediate base, on whose lower face polymer studs are arranged over the surface, which are integrally formed during the injection molding process. Examples of this are shown in U.S. Patent Nos. 5,929,516 and 6,249,048, whose disclosures are incorporated herein by reference thereto, and by the corresponding European Patent EP 0 782 765. These polymer studs are provided with an end surface which can be soldered and form external connections which are connected via integrated conductor runs to internal connections for the semiconductor component which is arranged on the substrate. The polymer studs are used as spacers for the module from a printed circuit board and are, thus, able to compensate for different expansion levels between the printed circuit board and the intermediate base. Contact can be made with the semiconductor component on the upper face of the intermediate base via bonding wires; however, a form of contact making is also feasible in which the different thermal coefficients of expansion are compensated for in an analogous manner via polymer studs on the upper face of the intermediate base.

In addition, a single-chip module is know from U.S. Patent No. 5,069,626, whose disclosure is incorporated herein by reference thereto, and from WO 89/00346. As disclosed by these references the injection-molded three-dimensional substrate composed of an electrically insulating polymer has integrally formed polymer studs on the lower face which are arranged in one row or in a number of rows along the circumference of the substrate. One chip is arranged on the upper face of the substrate and contact is made with it via fine bonding wires and conductor tracks, which are then, themselves, connected via plated through-holes to the external connections formed on the lower-face studs. In this embodiment, the intermediate base has a relatively large extent.

SUMMARY OF THE INVENTION

The object of the present invention is to provide an intermediate base for a semiconductor module, a production method for forming the intermediate base and a module in which contact can be made directly with the semiconductor component without any underfilling on the intermediate base and contact can be made with the intermediate base on the circuit carrier or base without any additional measures, and in which the different coefficients of expansion of the materials that are used do not have any apparent disadvantageous effect. In this case, the semiconductor component together with the intermediate base are intended to produce a module with a very compact physical form.

According to the invention, the first part of the object is achieved by an intermediate base for a module having at least one semiconductor component. The base comprises a flat base body having an upper face on which internal connections are formed for connection to component connecting elements of a semiconductor component, a lower face, which is provided with external connections for making contact with a circuit carrier, and through-holes between the upper face and the lower face, whose walls are at least partially metallized, and each makes a conductive connection between a contact point on the upper face and a corresponding external connection on the lower face, with the walls of the through-holes being at least partially exposed in the region of the lower face of the base body by means of

annular notches or grooves, which are incorporated adjacent to a circumferential edge of the through-hole and form a freestanding stud as the external connection.

The production of the stud by means of notches or grooves on the lower face of the intermediate base, as provided according to the invention, results in them being arranged recessed in the lower face surface and not projecting, or only their metallized layers project beyond the surface. Nevertheless, the studs are able to absorb and to compensate for temperature-dependent different expansion levels of the intermediate base, on the one hand, and on the circuit carrier or board, on the other hand. Contact is made via a short route through the metallized holes which run within the polymer stud to the upper face of the intermediate base, where the semiconductor component or else a number of semiconductor components is/are arranged, and contact is made with the internal connections.

The through-holes are preferably formed concentrically within the studs, so that the latter has a tubular or chimney-like configuration. However, an eccentric arrangement between the through-holes and the stud is also feasible, so that the latter approximately has the form of a tubular segment.

A particularly compact construction can be achieved if the intermediate base according to the invention is formed by a film composed of a plastic material, whose coefficient of expansion is approximately the same as that of the semiconductor component, which is generally silicon. In this case, the semiconductor component can be placed with its component connecting elements directly onto the internal connections on the upper face of the through-holes and can make contact therewith. This means that no connecting conductors whatsoever in the form of bonding wires or conductor tracks are required on the upper face of the intermediate base. Compensation for different thermal coefficients of expansion is then essentially required only between the intermediate base and the circuit carrier or board, and this compensation is provided via the polymer studs, which are provided according to the invention in the lower face area of the intermediate base.

subt A1 > ~~A film composed of LCP (Liquid Crystal Polymer) or a material with similar~~ thermal expansion characteristics is highly suitable for use as a material for the intermediate base. This material is described, for example, in the Journal Advancing Microelectronics, July/August ~~1998, page 15-18~~.

In a more preferred refinement, the external connecting elements are formed by a metal layer on the outer rim of the studs, which is in the form of a continuation of the metallization of the through-hole. This can be provided with an additional solder layer and the through-holes in the interior of the studs can also be filled with solder material.

In one particularly advantageous refinement of the invention, the internal connections are each only in the form of a continuation of the metallization of the inner walls of the through-hole, and this continuation covers the upper face opening of the respective through-hole. In this case, the metallization layer which forms the internal connection is applied directly to the component connecting elements of the already-fitted semiconductor component through the through-holes from the lower face of the intermediate base.

The method according to the present invention for producing a connecting base of at least one semiconductor component comprises the steps of the connecting side of the semiconductor component is fixed on an upper surface of a flat base body so that its component connections rest on the upper face of the base body, through-holes are drilled through the base body from the lower face as far as the upper face in order to expose the component connecting elements of the semiconductor component, the inner walls of the through-holes and the exposed contact surfaces of the semiconductor component are coated with a metal layer at the same time as at least part of the lower face of the base body, and the rim of the holes on the lower face of the base body is at least partially exposed by means of a circumferential notch.

The annular notches for exposing the hole rims are preferably produced in the same way as the holes for the through-holes, by means of a laser processing. In this case, further laser structuring for a conductor track structure can be carried out at the same time on the lower

face of the base body. During this processing step, those metal surfaces which are not required are removed and the remaining metal surfaces may be provided with an additional metal layer. In order to produce a greater thickness, additional solder layers, such as tin-lead, can be applied to these metal structures for soldering, so that there is no need for a process of paste printing.

However, a somewhat different method sequence is also feasible in which the studs on the lower face of the base body are produced even before the connection to the semiconductor component. In this case, the studs can be produced both by laser structuring and by stamping on the lower face of the base body. In this case, the semiconductor component would be fitted onto the base body provided with the studs, and the drilling of the through-holes would then be carried out from the lower face through the already preformed studs to the upper face of the base body, followed by a subsequent metallization.

Other advantages and features of the invention will be readily apparent from the following description of the preferred embodiments, the drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-4 are cross-sectional views showing individual steps of producing the intermediate base with a semiconductor component, with Fig. 1 being a cross-sectional view after the component is connected on the base; Fig. 2 being a cross-sectional view showing the arrangement after forming the through-holes; Fig. 3 being a cross-sectional view of the arrangement after applying the metallizing layer; and Fig. 4 being a cross-sectional view of the arrangement after forming the notches;

Fig. 5 is a perspective view with portions broken away for purposes of illustration of a cutaway intermediate base; and

Fig. 6 is a cross-sectional view showing a mounting of the semiconductor module according to the present invention on a printed circuit board.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The principles of the present invention are particularly useful when incorporated in an intermediate base, generally indicated at 1 in Fig. 6, which supports a semiconductor component, such as a chip 2, on a printed circuit board 4.

To produce the intermediate base 1, a base body 10, which is formed from a LCP film with a similarly low coefficient of expansion to that of the semiconductor component is utilized. As is known, the thermal coefficient of expansion of LCP is similar to that of silicon, so that such a base body can be connected directly to the semiconductor without any risk of different expansion when subjected to thermal loads. As shown in Fig. 1, the base body 10 is connected via an intermediate adhesive layer 3 to a semiconductor chip 2, whose component connecting elements are in the form of metal pads 21 that face the base body 10. The adhesive layer 3 may have a thickness of 25µm to 50µm, for example, while the LCP film which forms the base body 10 may, for example, have a thickness of 100µm to 200µm. It is also feasible to use a multilayer film for the base 10 and a conductor track structure can also be provided between the layers of the base 10.

In a second processing step shown in Fig. 2, through-holes 11 are drilled from the lower face 10a of the base body to the upper face of the base body 10, to be precise, so that they each meet one of the flat component connecting elements 21. These connecting elements 21 are thus exposed. The drilling process is carried out using a laser drilling method with the laser beam being set so that the component connecting element 21 is not removed.

After forming the through-holes 11, the inner walls of the through-holes 11 are provided entirely or at least partially with a metal layer 12, and this metal layer is also deposited on the exposed component connecting element 21 without any discontinuity. The semiconductor chip 2 thus makes direct contact with the intermediate base. The application of the metallization 12 also allows the other areas of the lower face 10a of the base body 10 to be entirely or partially covered with a metal layer.

As illustrated in Fig. 4, annular notches or grooves 14 are now incorporated around each of the through-holes 11, which produce chimney-like studs 15, which are arranged recessed in the base body 10, so that they do not project beyond the lower face 10a. The rims of the studs are already covered with the metal layer 12, as a result of the previous metallization process, and can thus be used directly as external connections for making contact on a printed circuit board. The depth of the notches 14 is governed by the required thermal load capacity, since these studs 15 can now absorb and compensate for the loads that occur in the event of different thermal expansion of the intermediate base 1 with the semiconductor chip 2 seated on it and with the printed circuit board.

The notches 14 are ideally arranged concentrically with respect to the through-holes 11, so that the studs 15 have a symmetrically tubular shape. However, it is also feasible, for specific reasons or as a result of dimensional discrepancies, for a notch 16 (Fig. 4) to be located eccentrically with respect to the corresponding through-hole 11, thus resulting in a stud 17 which is cut on one side, in the form of an annular segment (see Figs. 4 and 5).

At the same time that the notches 14 are incorporated, a desired conducting structure can also be produced on the lower face of the base body 10 by laser processing during the same processing step. In this case, the metal surfaces which are not required can be removed and the remaining metal surfaces can be provided with an additional metal coating. Solder materials can be applied to the rims of the studs, which are used as external contacts 18, in order, in particular, to achieve a greater metal thickness.

As illustrated in Fig. 6, the invention makes contact with an intermediate base 1 and a semiconductor chip 2 on a printed circuit board 4, with the external contacts 18 each being reinforced by a solder layer 19 composed of tin-lead. Fig. 6 also shows that the tin-lead alloy 19 may fill one of the through-holes 11.

Although various minor modifications may be suggested by those versed in the art, it should be understood that I wish to embody within the scope of the patent granted hereon all such modifications as reasonably and properly come within the scope of my contribution to the art.